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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/814,312

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Bradley C. Aldrich

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EXAMINER

LINDLOF, JOHN M

ART UNIT

PAPER NUMBER

2183

NOTIFICATION DATE

DELIVERY MODE

08/03/2010

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/814,312	<b>Applicant(s)</b> ALDRICH ET AL.	
	<b>Examiner</b> JOHN LINDLOF	<b>Art Unit</b> 2183	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 May 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)         | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

1. Claims 1-36 are presented for examination.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, and similarly claim 9, 14, 23, and 30, recites the limitation "the upper or lower unsigned data operands". There is insufficient antecedent basis for this limitation in the claim.

Claims 2-8, 10-13, 15-22, 24-29, 31-36 are rejected for being dependent, either directly or indirectly, upon a rejected independent claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 11-15, 17-24, 26-30, 32-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Grisenthwaite et al., US Patent Application Publication 2002/0065860 (hereinafter Grisenthwaite).

2. As per claim 1, Grisenthwaite teaches:

A method of executing an instruction comprising: receiving residual data of a first image and decoded pixels of a second image (examiner notes that the name of data received is not given much, if any, patentable weight because it has no effect on the process as claimed, Grisenthwaite teaches receiving residual and decoded data such as pixel/image data at para. [0129]); zero-extending a plurality of unsigned data operands (see e.g. fig. 4, 5, operands p0-3) of the decoded pixels using one or more qualifiers (see e.g. fig. 4, para. [0118], [0123], shift parameter) to determine whether the upper or lower unsigned data operands are operated on to produce a plurality of unpacked data operands (see e.g. fig. 4, 5, operands can be zero extended such as by sign/zero extending and masking circuit 10 to produce unpacked data; the shift parameter determines whether upper or lower operands are operated on as shown in fig. 4 with p3/p2 and p1/p0); adding a plurality of signed data operands of the residual data to the plurality of unpacked data operands producing a plurality of signed results

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(see e.g. para. [0129], values are added to produce results which can be signed); saturating the plurality of signed results producing a plurality of unsigned results (see e.g. para. [0129], signed results are then saturated to an unsigned result).

*\*Examiner's note\* A recitation of an intended use, such as processing data of a certain name or origin, must result in a structural or functional difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. The origin of bits of data, or the abstract name given to them, does not change the fact that the data are still a series of bits, and therefore the claimed method is taught by prior art which performs the claimed method on bits of data which are capable of representing an image, pixels, etc.. This interpretation of data is consistent with applicant's specification, which describes performing operations on bits of data (see e.g. page 12, "the residual data is typically 16-bit signed data", "...a previously decoded frame saturated to 8-bit unsigned limits).*

3. As per claim 2, Grisenthwaite teaches:

The method as recited in claim 1, wherein the residual data comprises data results from an inverse discrete cosine transform (DCT) operation and the second image comprises a previously decoded video frame (see e.g. para. [0129]).

4. As per claim 3, Grisenthwaite teaches:

The method as recited in claim 1, wherein the second image is an earlier decoded block from a same video frame as the first image (see e.g. para. [0129], the data is capable of being from any image).

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5. As per claim 4, Grisenthwaite teaches:

The method as recited in claim 1, wherein the zero-extending, the adding and the saturating are part of a video estimation function (see e.g. para. [0129], motion estimated value).

6. As per claim 5, Grisenthwaite teaches:

The method as recited in claim 1, wherein the zero-extending, the adding and the saturating are part of a video compensation function (see e.g. para. [0129], motion compensation).

7. As per claim 6, Grisenthwaite teaches:

The method as recited in claim 1, wherein the instruction is a Single-Instruction/Multiple-Data (SIMD) instruction (see e.g. para. [0014]).

8. As per claim 7, Grisenthwaite teaches:

The method as recited in claim 1, wherein the method comprises executing a Single-Instruction/Multiple-Data (SIMD) instruction (see e.g. para. [0014]).

9. As per claim 8, Grisenthwaite teaches:

The method as recited in claim 1, wherein the method is performed utilizing Single-Instruction/Multiple-Data (SIMD) circuitry (see e.g. para. [0014]).

10. Claims 9, 11-13 are rejected for reasons corresponding to those given above for claims 1-2, 5, 6.

11. Claims 14-15 are rejected for reasons corresponding to those given above for claim 1.

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12. As per claim 17, Grisenthwaite teaches:

The apparatus as recited in claim 14, wherein selection controls for the first plurality of multiplexers is according to a qualifier specified in a Single-Instruction/Multiple-Data (SIMD) instruction (see e.g. para. [0014]).

13. As per claim 18, Grisenthwaite teaches:

The apparatus as recited in claim 14, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction (see e.g. para. [0014], the type of instruction causes certain units to be used).

14. As per claim 19, Grisenthwaite teaches:

The apparatus as recited in claim 14, wherein configuration of the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction (see e.g. para. [0014], the type of instruction causes certain units to be used).

15. As per claim 20, Grisenthwaite teaches:

The apparatus as recited in claim 14, wherein the first plurality of multiplexers, the plurality of adders, and the plurality of saturation units form a Single-Instruction/Multiple-Data (SIMD) instruction execution circuit (see e.g. para. [0014]).

16. Claims 21-22 are rejected for reasons corresponding to those given above for claims 2, 5.

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17. Claims 23, 24, 26-29 are rejected for reasons corresponding to those given above for claims 14, 15, 17-22.

18. Claims 30, 32-36 are rejected for reasons corresponding to those given above for claims 14, 15, 17-22.



***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grisenthwaite in view of Paver, US Patent Application Publication 2002/0083311 (hereinafter Paver).

19. As per claim 10, Grisenthwaite fails to explicitly teach performing an OR operation on the result data, and storing the result data in a single register.

Paver teaches performing an OR operation on data and storing it in a single register (see e.g. fig. 5)

Grisenthwaite teaches performing OR operations (see e.g. fig. 3C OR gates).

Examiner asserts the performing an OR operation on two data elements is extremely common in the art. At the time of the invention it would have been obvious to one of ordinary skill in the art to combine the teachings of Grisenthwaite and Paver to perform an OR operation on two data elements and store the result in a single register. This would have incorporated the known functionality of performing an OR operation in order to achieve the predictable result of creating a value given by the result of performing an OR operation on two elements.

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20. Claims 16, 25, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grisenthwaite in view of Paver, US Patent Application Publication 2002/0083311 (hereinafter Paver).

21. As per claim 16, Grisenthwaite teaches:

The apparatus as recited in claim 14,

Grisenthwaite fails to explicitly teach wherein the plurality of adders comprises four 16-bit adders.

Nojiri teaches a plurality of adders as four 16-bit adders (see e.g. col. 3 lines 43-50).

Grisenthwaite teaches performing add operations (see e.g. fig. 4).

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine the teachings of Grisenthwaite and Nojiri to use a plurality of adders as four 16-bit adders. This would have incorporated the known functionality of performing an add operation on known 16-bit data to achieve the predictable result of adding four sets of 16-bit values.

22. Claims 25, 31 are rejected for reasons corresponding to those given above for claim 16.

***Response to Arguments***

Applicant's arguments filed 5/3/2010 have been fully considered but they are not persuasive.

Applicant states: "Claim 1 teaches zero-extending a plurality of unsigned data operands of the decoded pixels using qualifiers to determine whether the upper or lower unsigned data operands are operated on. Nowhere does Grisenthwaite teach using qualifiers to determine whether the upper or lower unsigned data operands are operated on. Consequently, Grisenthwaite fails to provide an identical disclosure of at least this element of the claimed subject matter."

Examiner respectfully disagrees. Grisenthwaite teaches using a qualifier as a shift parameter (see e.g. fig. 4, para. [0118], [0123], shift parameter). This shift parameter qualifier is used to determine which upper or lower data operands are operated on as discussed in para. [0118]: "Depending upon whether or not a rotate right operation of 8-bit positions is specified in the instruction, either the multibit portions p0 and p2 or alternatively the multibit portions p1 and p3 are selected out of the input data word within register Rm."

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LINDLOF whose telephone number is (571)270-1024. The examiner can normally be reached on Monday-Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/  
Supervisory Patent Examiner, Art Unit 2183

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